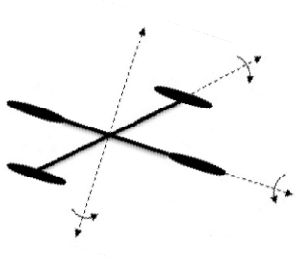
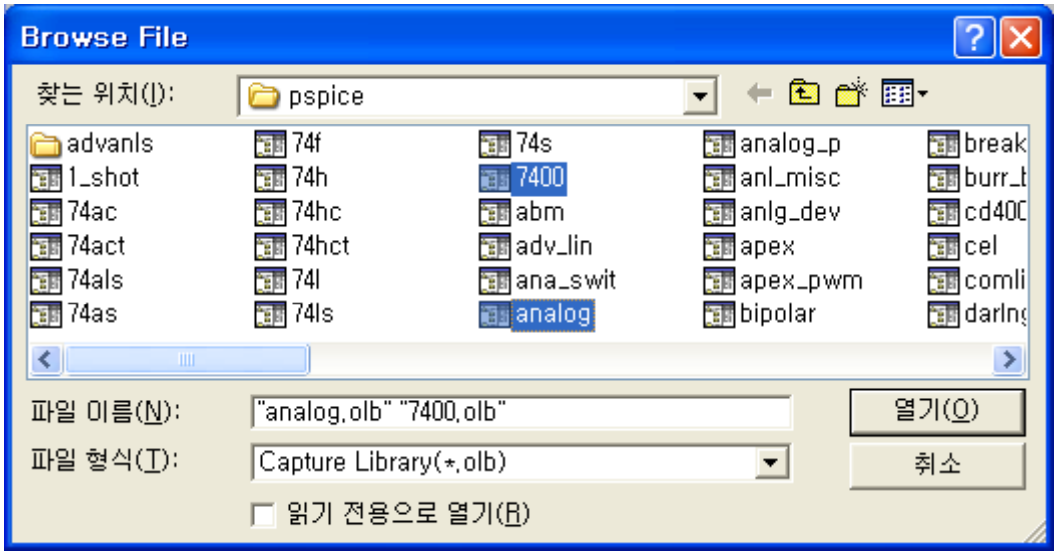
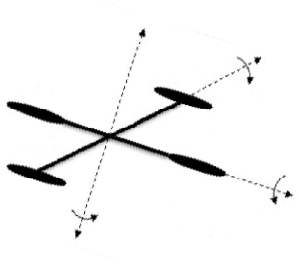
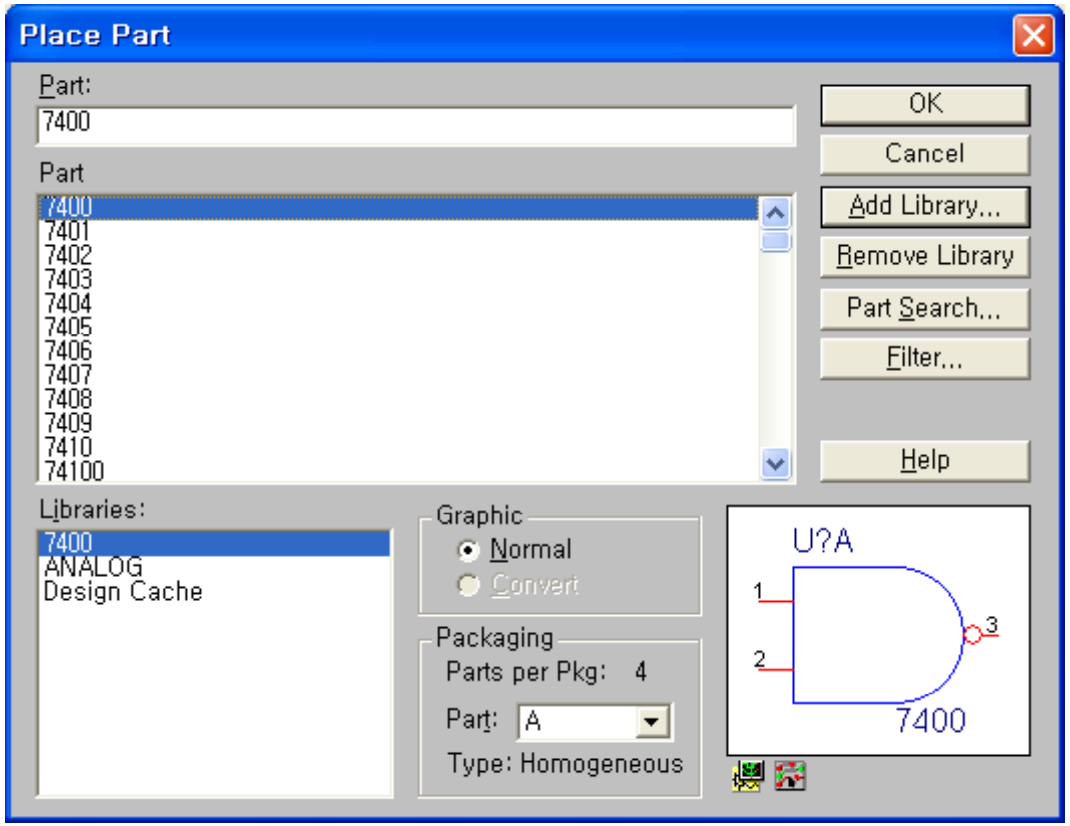
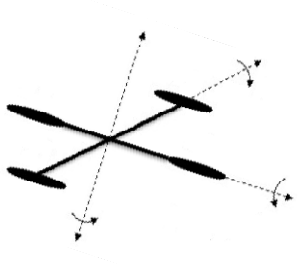
2. 간단한 디지털 회로 시뮬레이션 하기

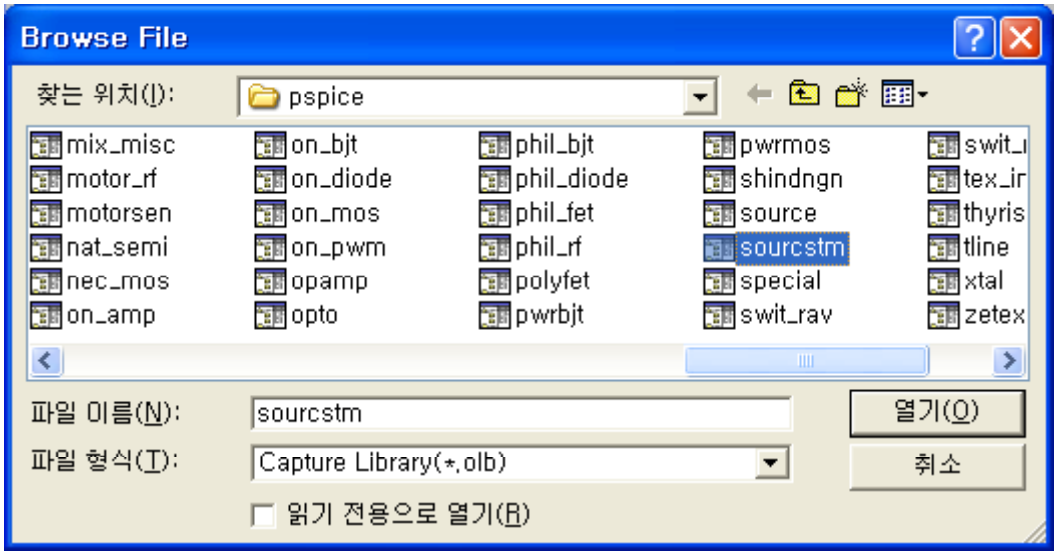


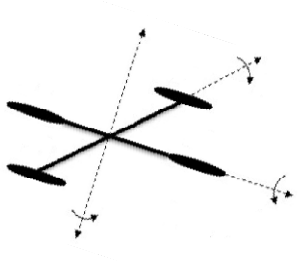

Browse File
찾는 위치(I):
pspice
advanls
1_shot
74ac
74act
74als
74as
74f
74h
74hc
74hct
74l
74ls
74s
7400
abm
adv_lin
ana_swit
analog
analog_p
anl_misc
anlg_dev
apex
apex_pwm
bipolar
break
burr_b
cd40C
cel
comli
darlng
파일 이름(N):
"analog.olb" "7400.olb"
열기(O)
파일 형식(T):
Capture Library(*.olb)
취소
읽기 전용으로 열기(R)

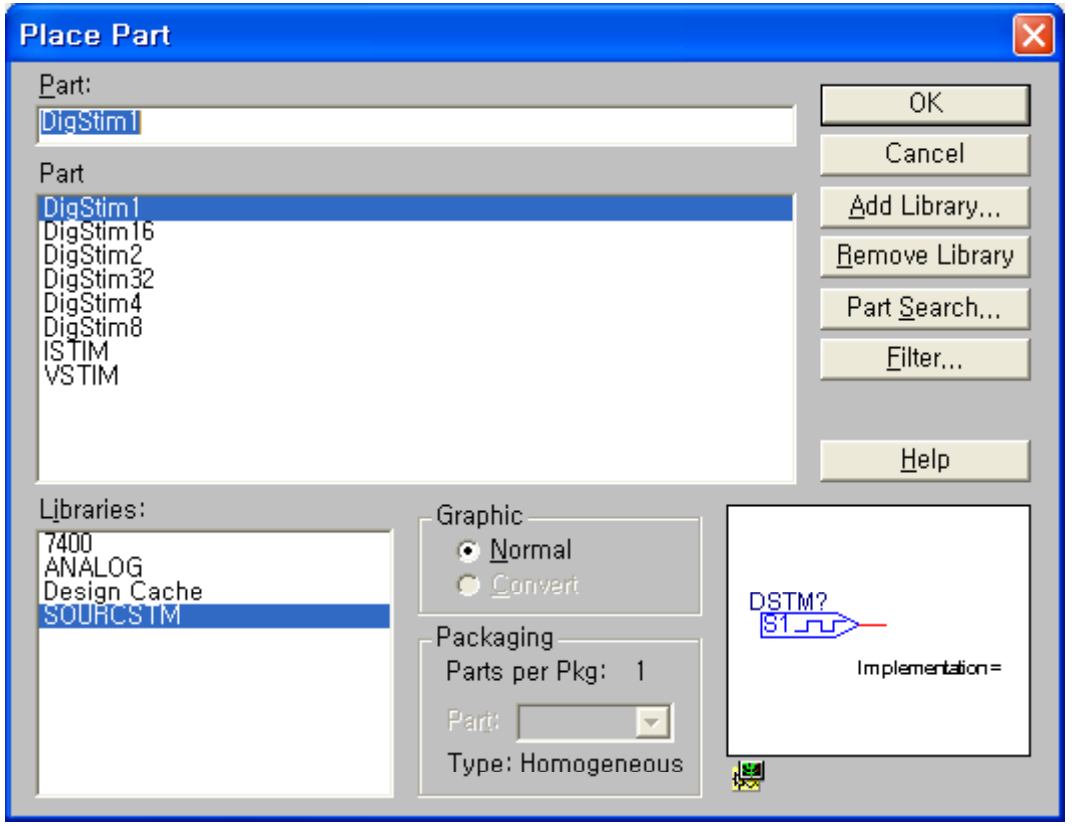


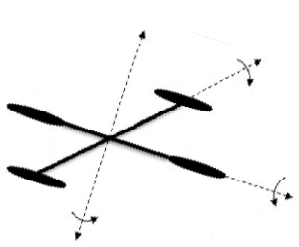

Place Part
Part:
7400
Part
7400
7401
7402
7403
7404
7405
7406
7407
7408
7409
7410
74100
OK
Cancel
Add Library...
Remove Library
Part Search...
Filter...
Help
Libraries:
7400
ANALOG
Design Cache
Graphic
Normal
Convert
Packaging
Parts per Pkg: 4
Part: A
Type: Homogeneous
U?A
1
2
3
7400

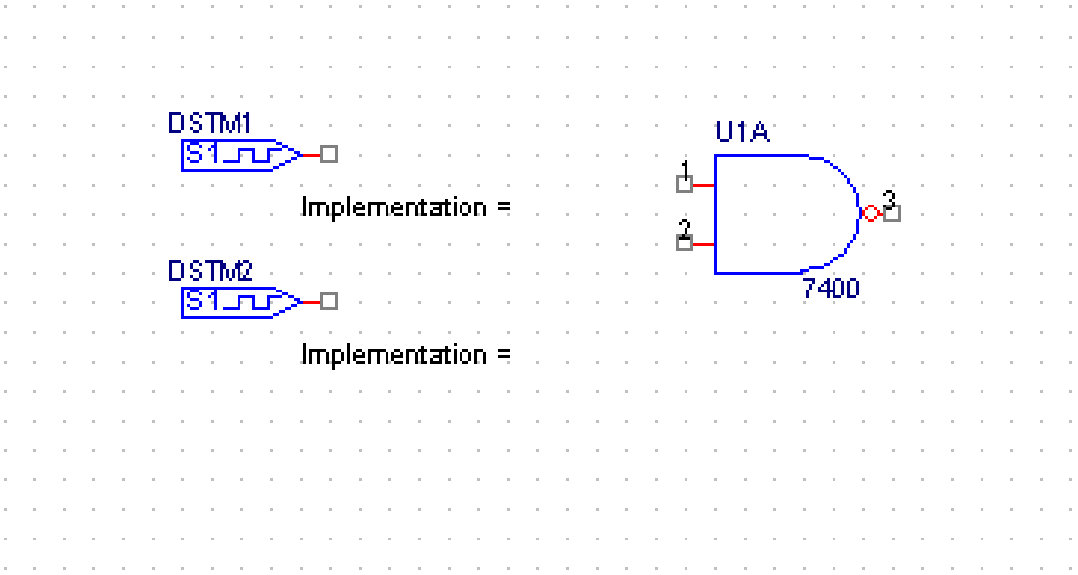


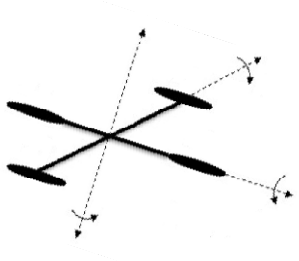

Browse File
찾는 위치(I):
pspice
mix_misc
motor_rf
motorsen
nat_semi
nec_mos
on_amp
on_bjt
on_diode
on_mos
on_pwm
opamp
opto
phil_bjt
phil_diode
phil_fet
phil_rf
polyfet
pwrbjt
pwrmos
shindngn
source
sourcstm
special
swit_rav
swit_ı
tex_ir
thyris
tline
xtal
zetex
파일 이름(N):
sourcstm
열기(O)
파일 형식(T):
Capture Library(*.olb)
취소
읽기 전용으로 열기(R)

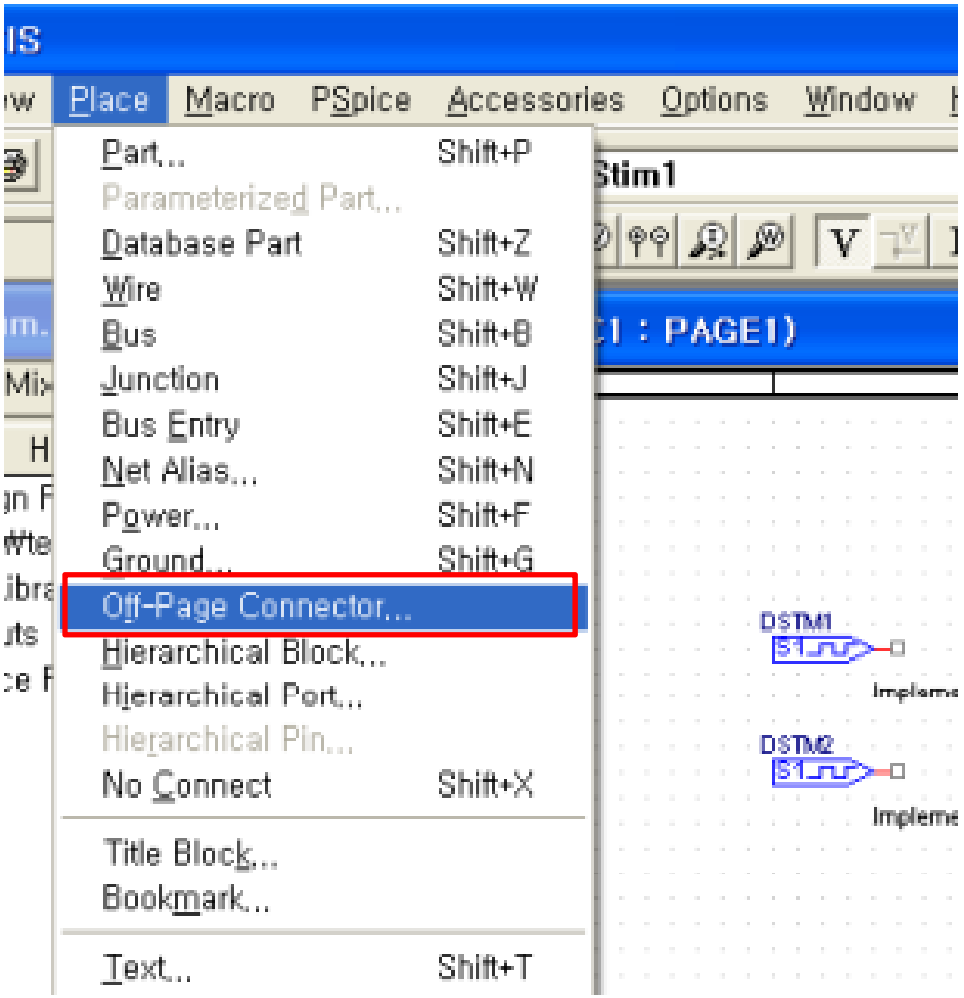


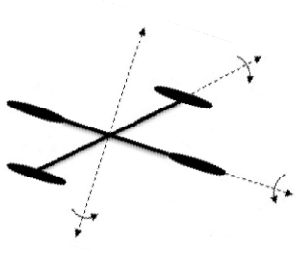

Place Part
Part:
DigStim1
Part
DigStim1
DigStim16
DigStim2
DigStim32
DigStim4
DigStim8
ISTIM
VSTIM
OK
Cancel
Add Library...
Remove Library
Part Search...
Filter...
Help
Libraries:
7400
ANALOG
Design Cache
SOURCSTM
Graphic
Normal
Convert
Packaging
Parts per Pkg: 1
Part:
Type: Homogeneous
DSTM?
S1
Implementation=

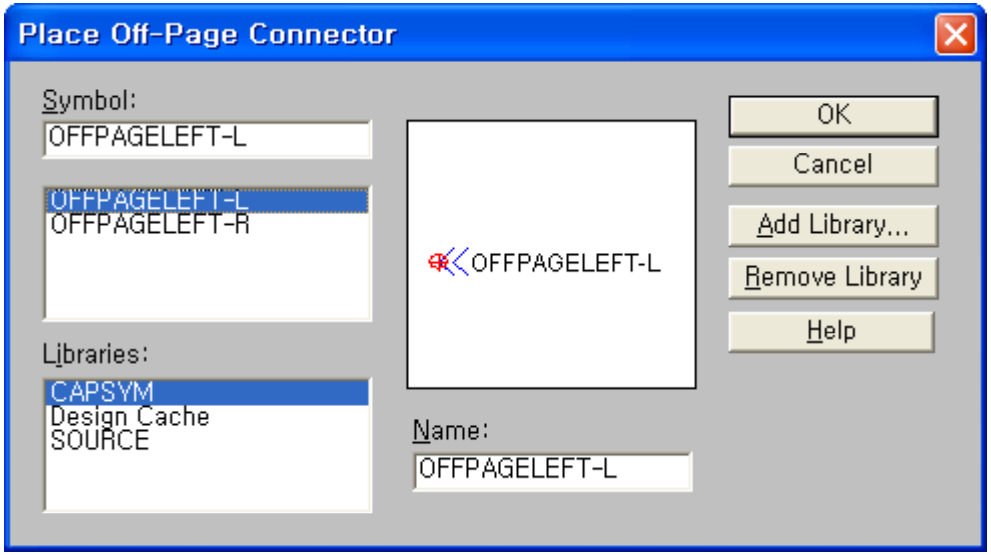


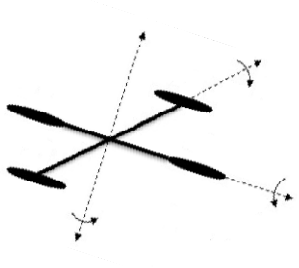

DSTM1
S1
Implementation =
DSTM2
S1
Implementation =
U1A
1
2
3
7400

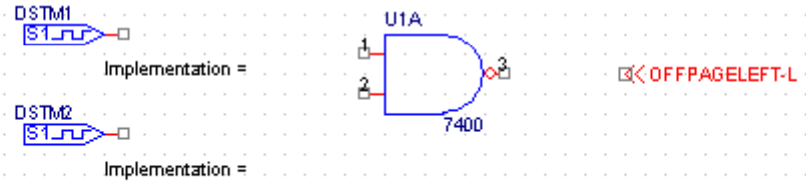


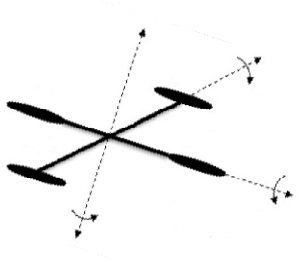

Place
Macro
PSpice
Accessories
Options
Window
Part... Shift+P
Parameterized Part...
Database Part Shift+Z
Wire Shift+W
Bus Shift+B
Junction Shift+J
Bus Entry Shift+E
Net Alias... Shift+N
Power... Shift+F
Ground... Shift+G
Off-Page Connector...
Hierarchical Block...
Hierarchical Port...
Hierarchical Pin...
No Connect Shift+X
Title Block...
Bookmark...
Text... Shift+T
Stim1
DSTM1
DSTM2

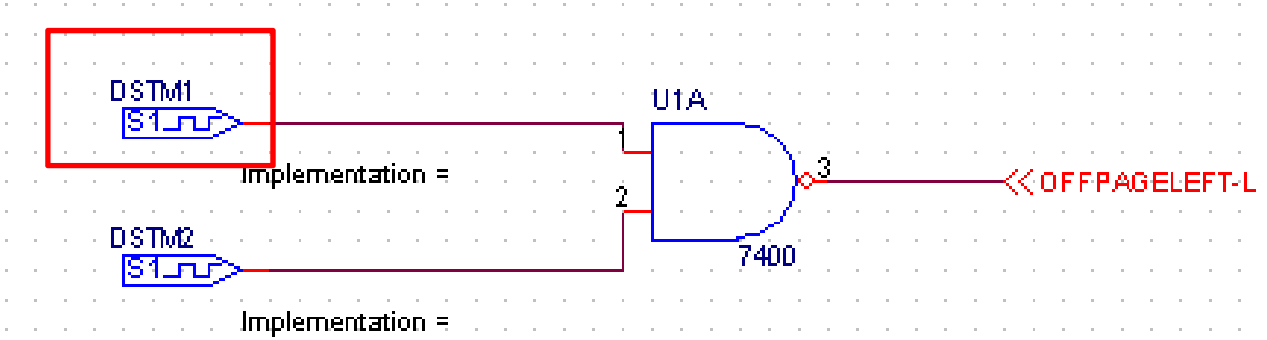


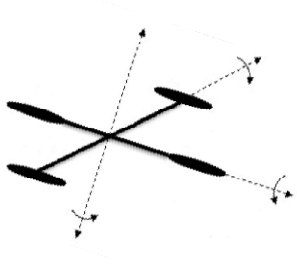

Place Off-Page Connector
Symbol:
OFFPAGELEFT-L
OFFPAGELEFT-L
OFFPAGELEFT-R
Libraries:
CAPSYM
Design Cache
SOURCE
OFFPAGELEFT-L
Name:
OFFPAGELEFT-L
OK
Cancel
Add Library...
Remove Library
Help

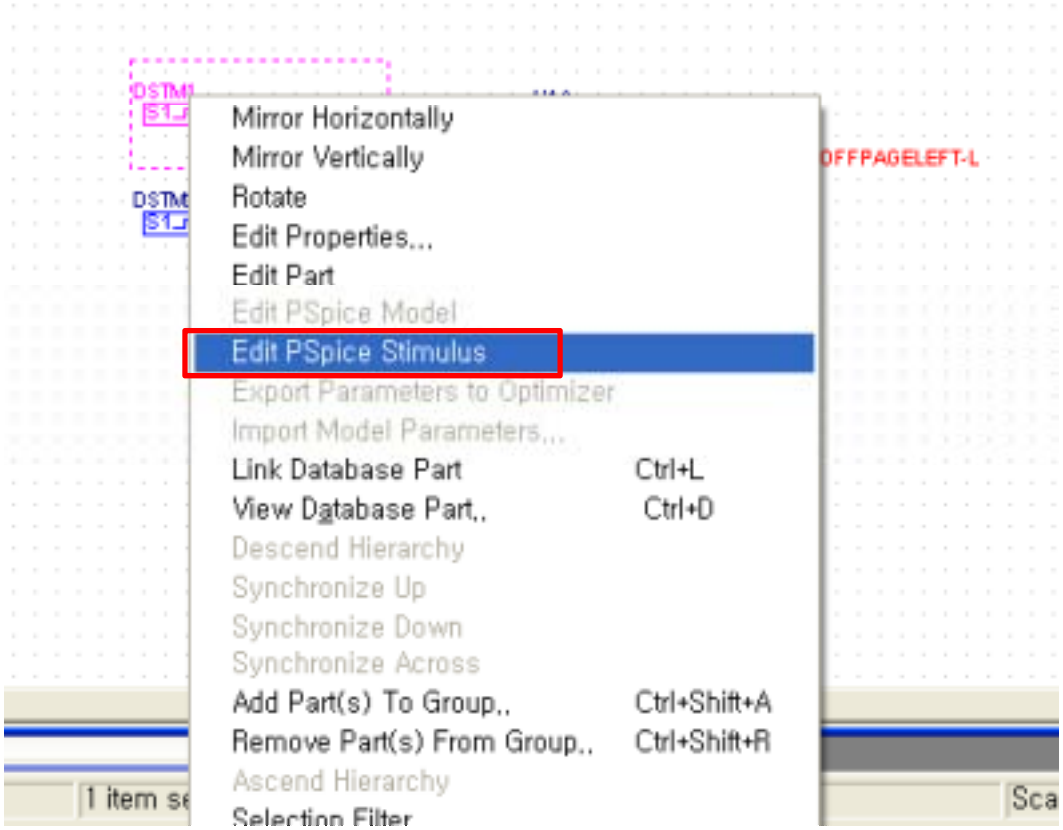


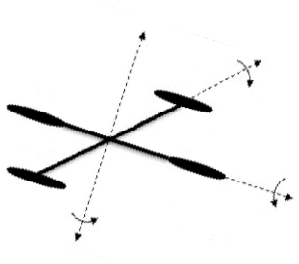

DSTM1
S1
Implementation =
DSTM2
S1
Implementation =
U1A
1
2
3
7400
OFFPAGELEFT-L

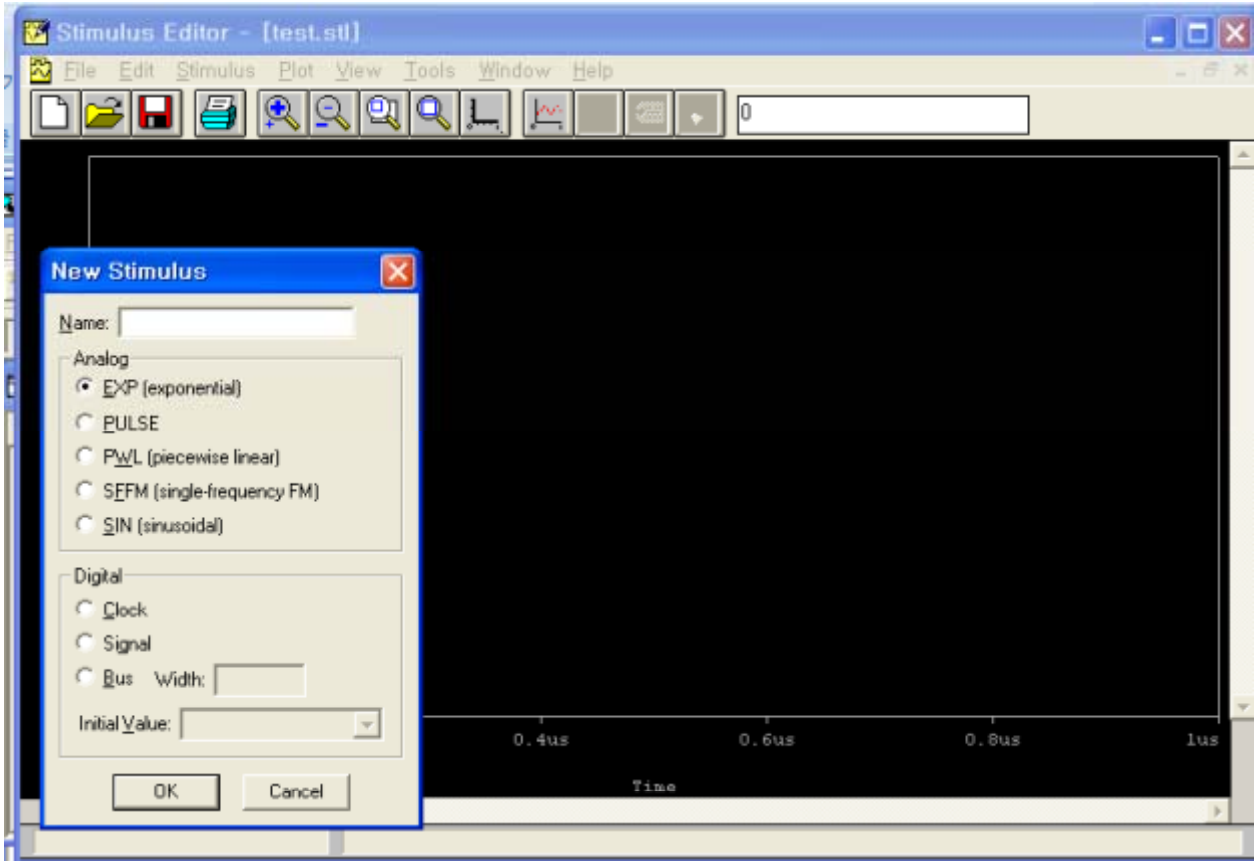


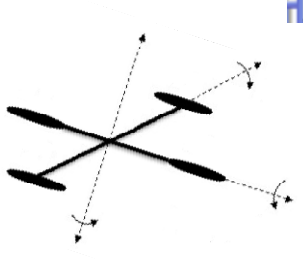

DSTM1
S1
Implementation =
DSTM2
S1
Implementation =
U1A
1
2
3
7400
OFFPAGELEFT-L

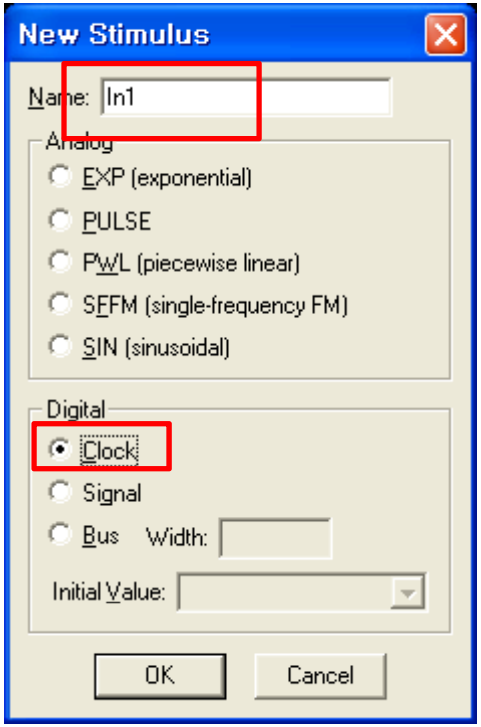


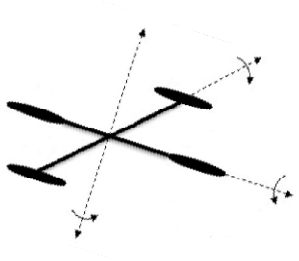

Mirror Horizontally
Mirror Vertically
Rotate
Edit Properties...
Edit Part
Edit PSpice Model
Edit PSpice Stimulus
Export Parameters to Optimizer
Import Model Parameters...
Link Database Part Ctrl+L
View Database Part,. Ctrl+D
Descend Hierarchy
Synchronize Up
Synchronize Down
Synchronize Across
Add Part(s) To Group,. Ctrl+Shift+A
Remove Part(s) From Group,. Ctrl+Shift+R
Ascend Hierarchy
Selection Filter
OFFPAGELEFT-L

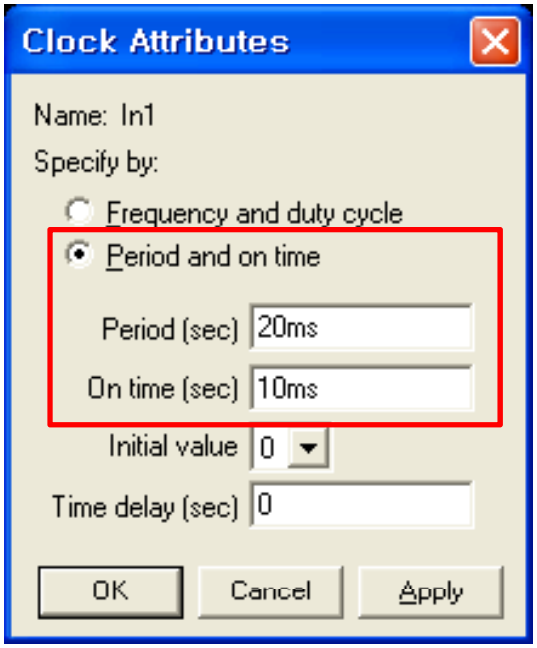


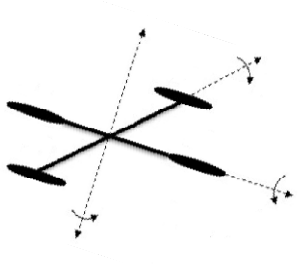

Stimulus Editor - [test.stl]
File Edit Stimulus Plot View Tools Window Help
0
New Stimulus
Name:
Analog
EXP (exponential)
PULSE
PWL (piecewise linear)
SFFM (single-frequency FM)
SIN (sinusoidal)
Digital
Clock
Signal
Bus Width:
Initial Value:
OK
Cancel
0.4us
0.6us
0.8us
1us
Time

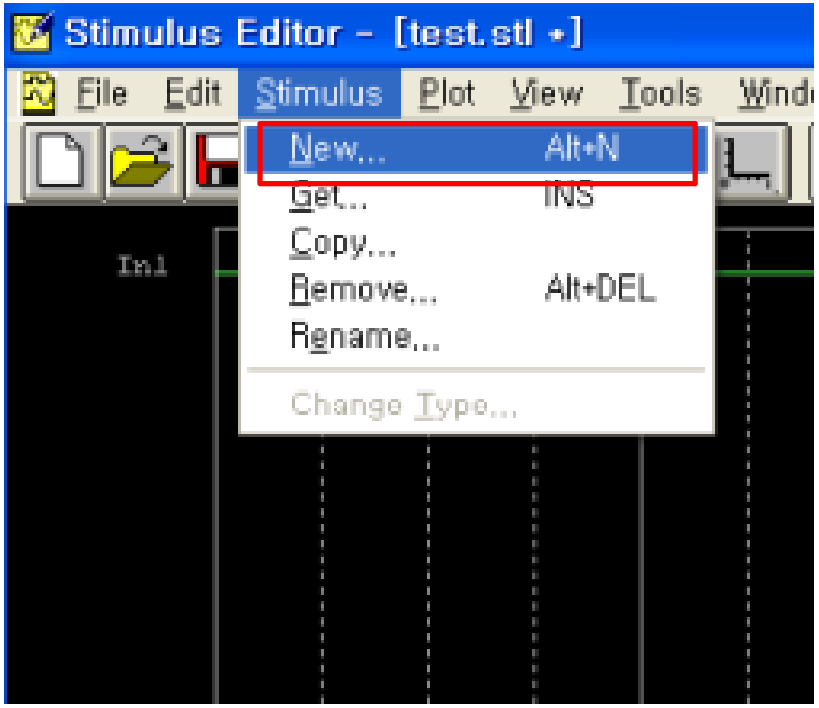


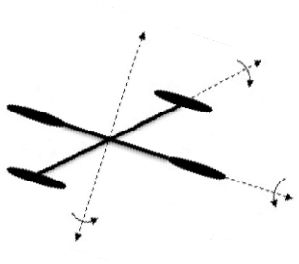

New Stimulus
Name: In1
Analog
EXP (exponential)
PULSE
PWL (piecewise linear)
SFFM (single-frequency FM)
SIN (sinusoidal)
Digital
Clock
Signal
Bus Width:
Initial Value:
OK
Cancel

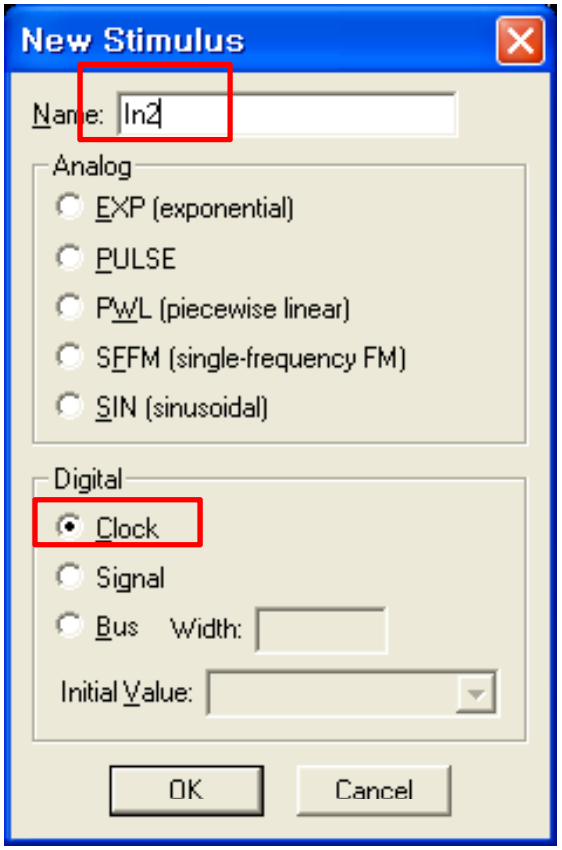


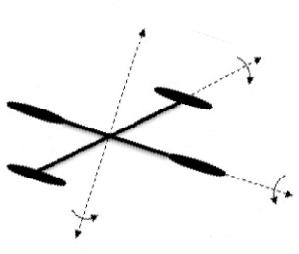

Clock Attributes
Name: In1
Specify by:
Frequency and duty cycle
Period and on time
Period (sec) 20ms
On time (sec) 10ms
Initial value 0
Time delay (sec) 0
OK
Cancel
Apply

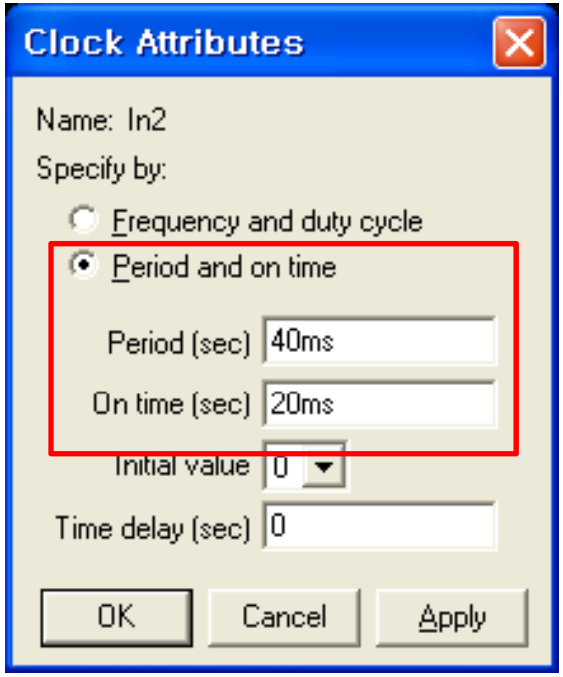


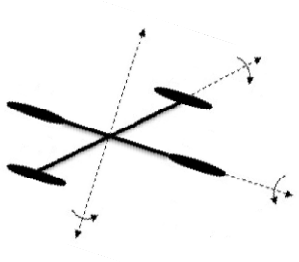

Stimulus Editor - [test.stl *]
File
Edit
Stimulus
Plot
View
Tools
New... Alt+N
Get... INS
Copy...
Remove... Alt+DEL
Rename...
Change Type...

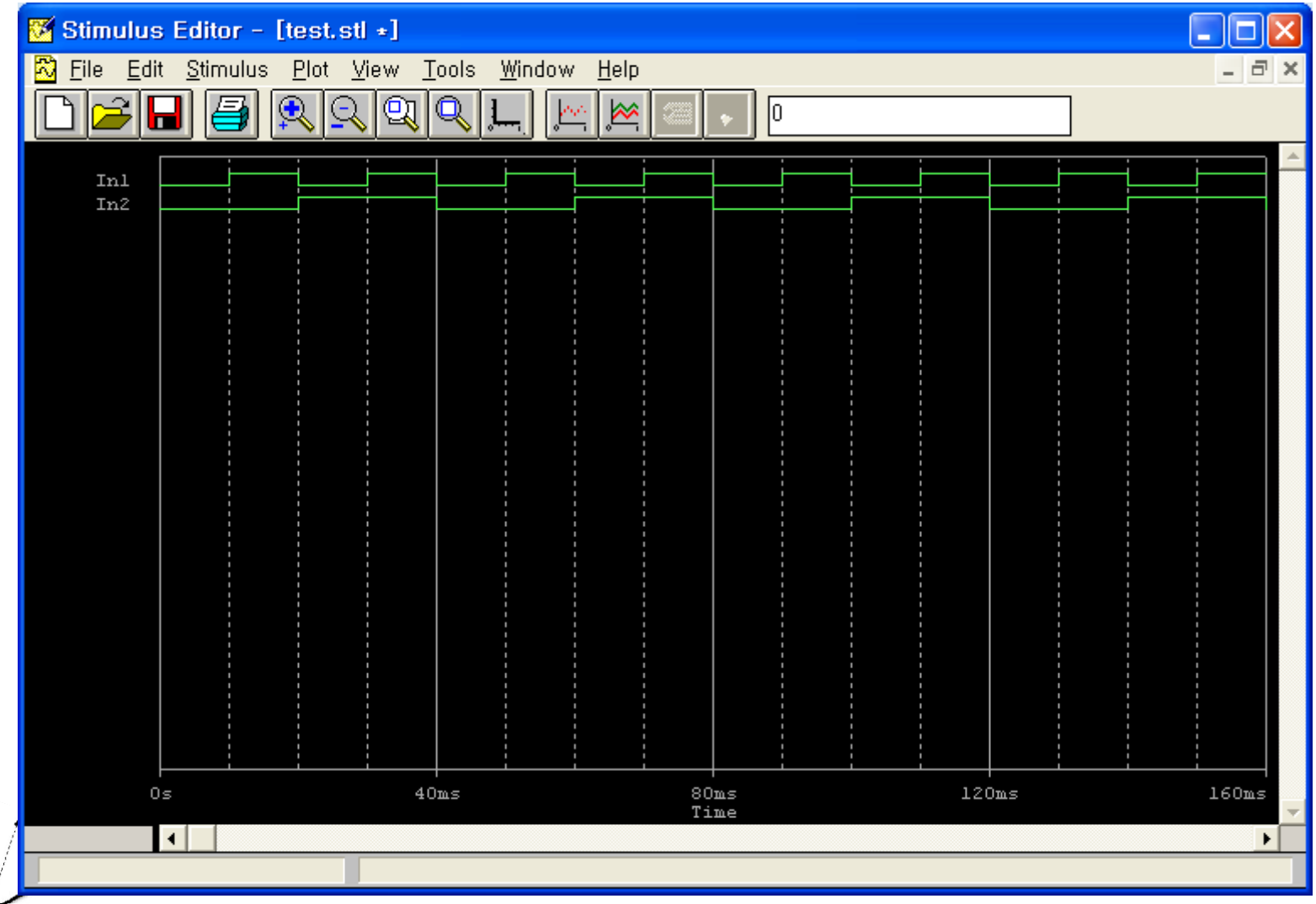


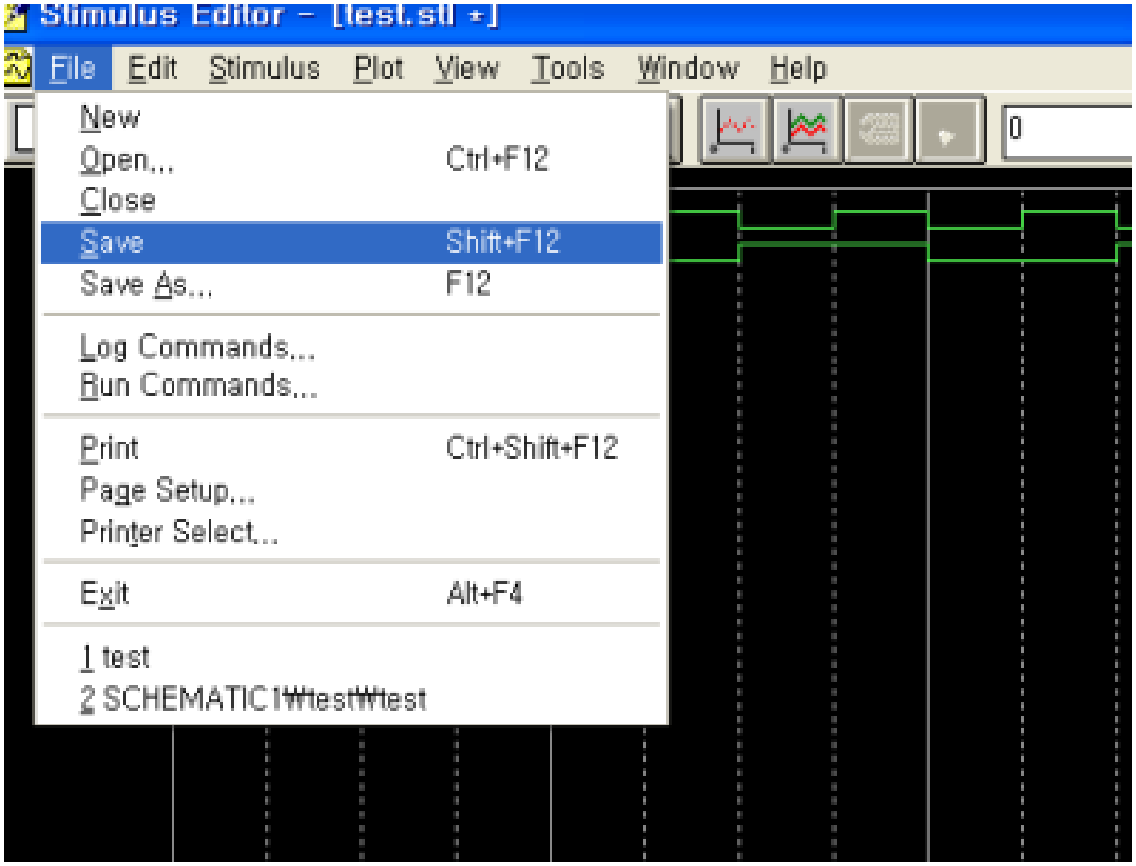

New Stimulus
Name: In2
Analog
EXP (exponential)
PULSE
PWL (piecewise linear)
SFFM (single-frequency FM)
SIN (sinusoidal)
Digital
Clock
Signal
Bus Width:
Initial Value:
OK
Cancel

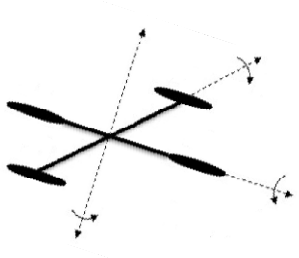


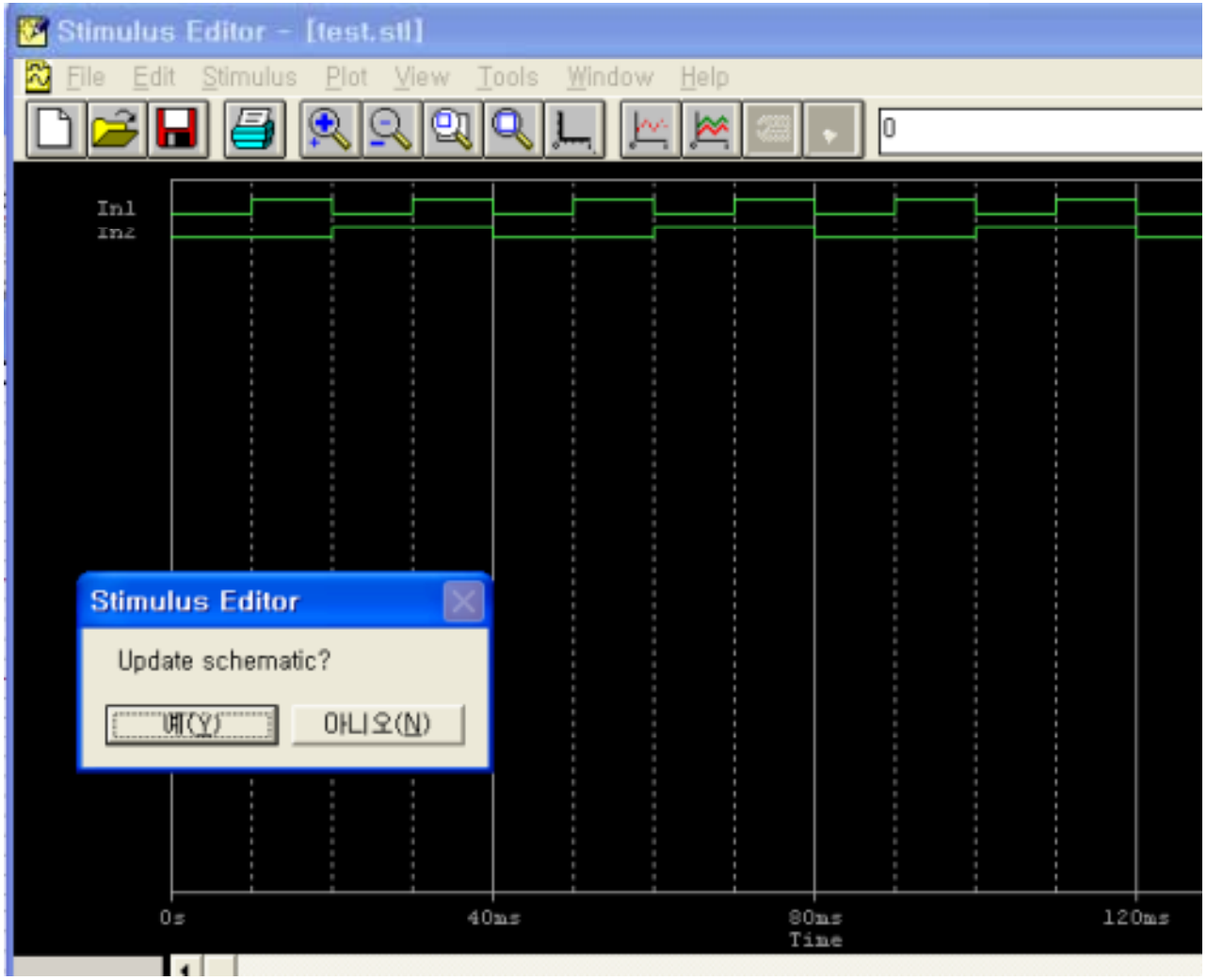

Clock Attributes
Name: In2
Specify by:
Frequency and duty cycle
Period and on time
Period (sec) 40ms
On time (sec) 20ms
Initial value 0
Time delay (sec) 0
OK
Cancel
Apply

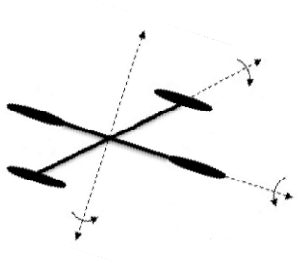


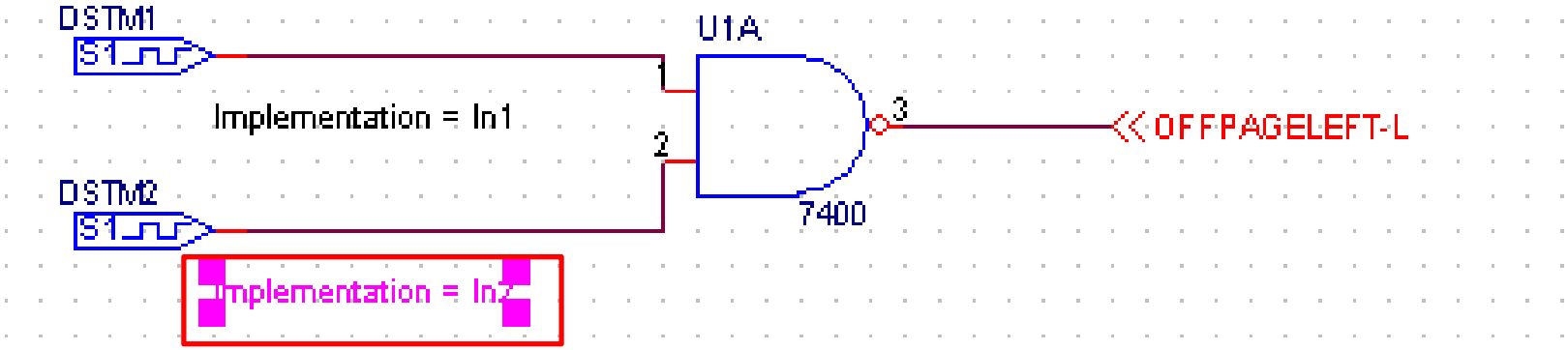

Stimulus Editor - [test.stl *]
File Edit Stimulus Plot View Tools Window Help
0
In1
In2
0s
40ms
80ms
120ms
160ms
Time

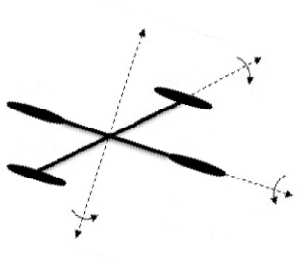

Stimulus Editor - [test.stl *]
File Edit Stimulus Plot View Tools Window Help
New
Open... Ctrl+F12
Close
Save Shift+F12
Save As... F12
Log Commands...
Run Commands...
Print Ctrl+Shift+F12
Page Setup...
Printer Select...
Exit Alt+F4
1 test
2 SCHEMATIC1₩test₩test
0

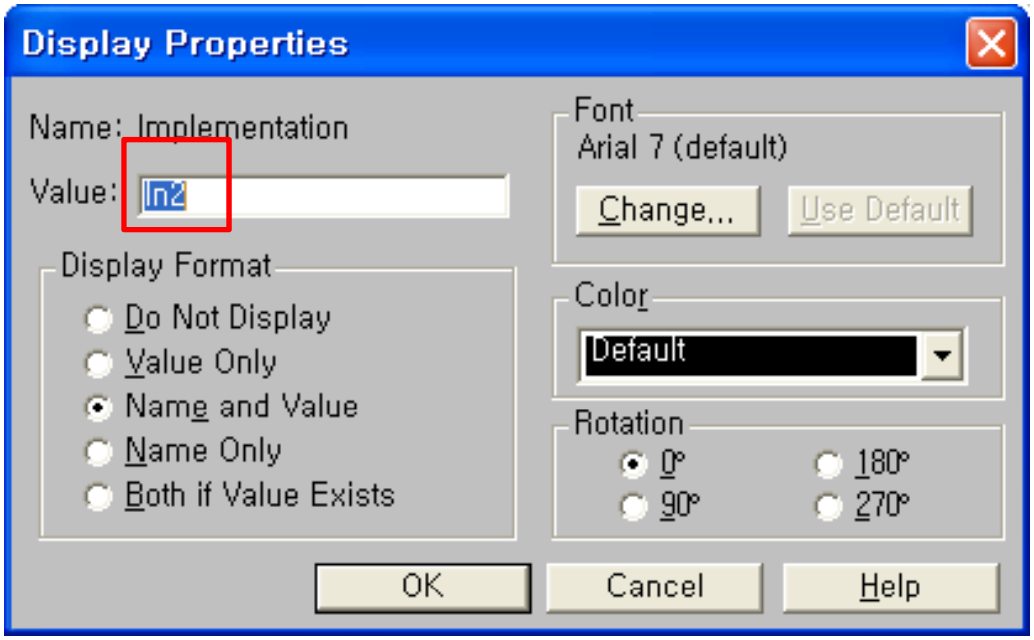


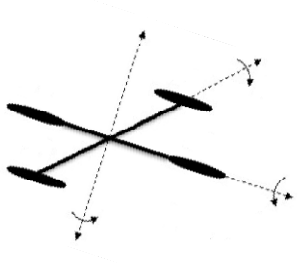

Stimulus Editor - [test.stl]
File Edit Stimulus Plot View Tools Window Help
0
In1
In2
Stimulus Editor
Update schematic?
예(Y)
아니오(N)
0s
40ms
80ms
120ms
Time

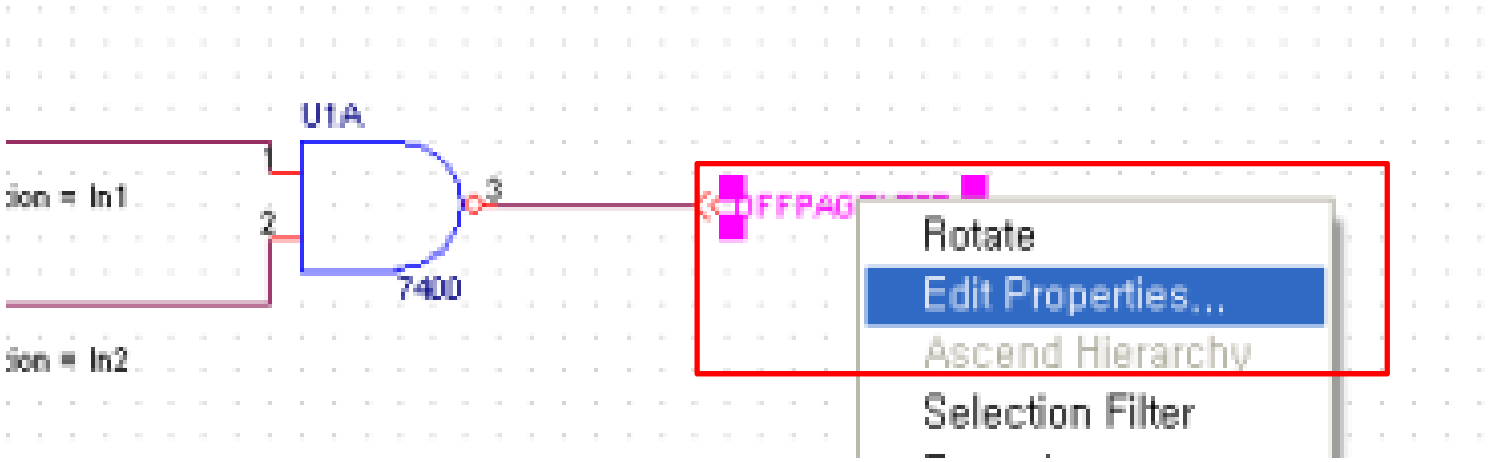


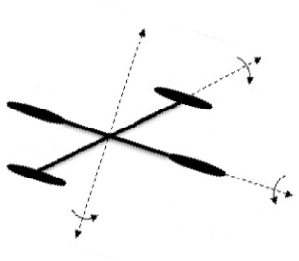

DSTM1
S1
Implementation = In1
DSTM2
S1
Implementation = In2
U1A
1
2
3
7400
OFFPAGELEFT-L

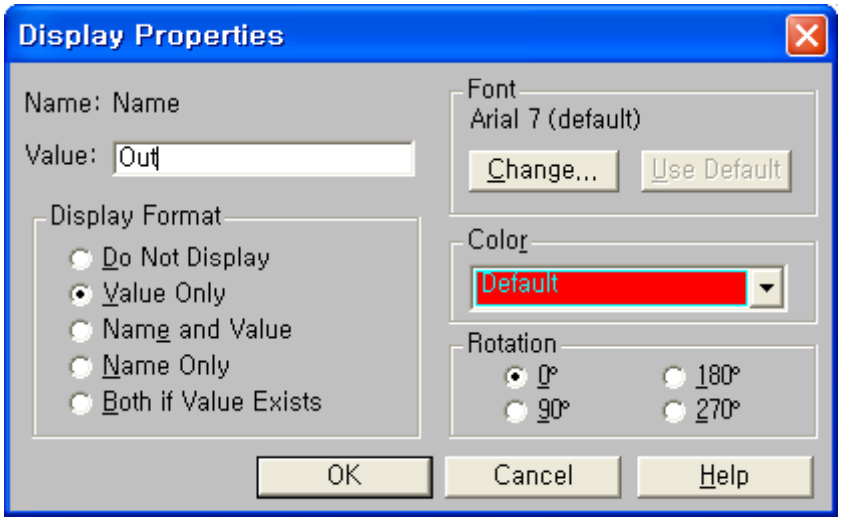


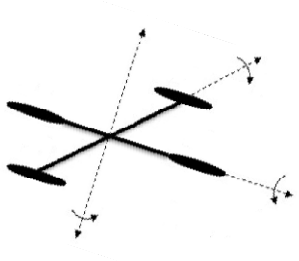

Display Properties
Name: Implementation
Value: In2
Font
Arial 7 (default)
Change...
Use Default
Display Format
Do Not Display
Value Only
Name and Value
Name Only
Both if Value Exists
Color
Default
Rotation
0°
180°
90°
270°
OK
Cancel
Help

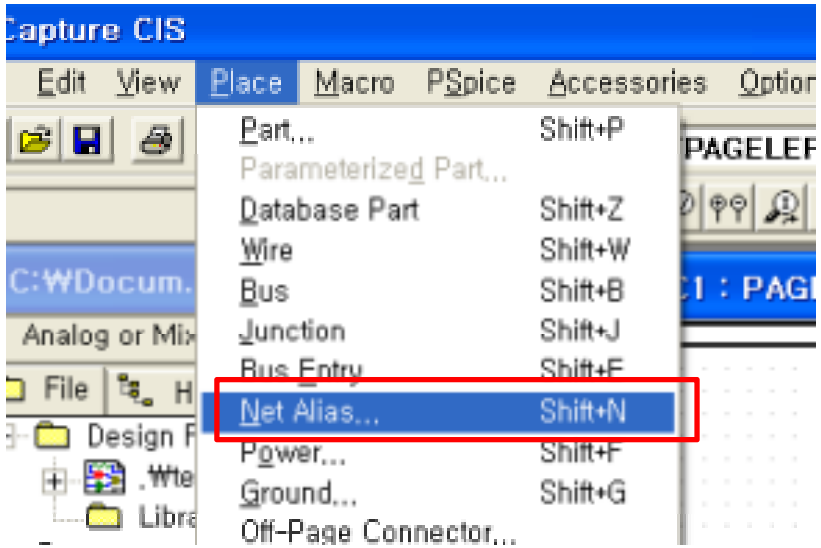



U1A
1
2
3
7400
Rotate
Edit Properties...
Ascend Hierarchy
Selection Filter

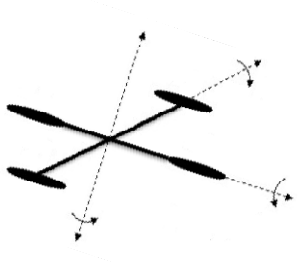


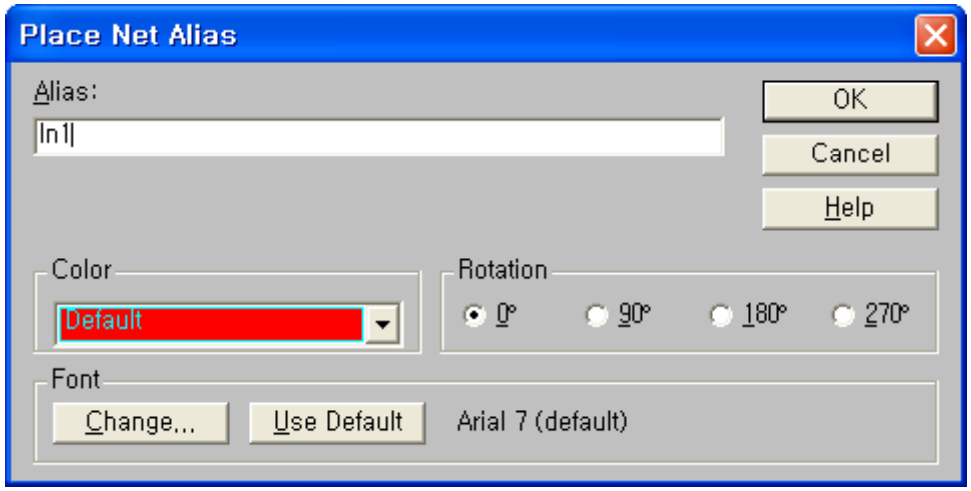

Display Properties
Name: Name
Value: Out
Font
Arial 7 (default)
Change...
Use Default
Display Format
Do Not Display
Value Only
Name and Value
Name Only
Both if Value Exists
Color
Default
Rotation
0°
180°
90°
270°
OK
Cancel
Help

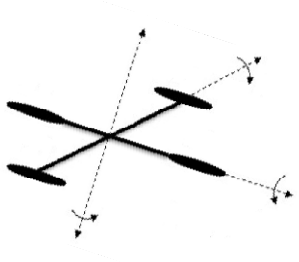


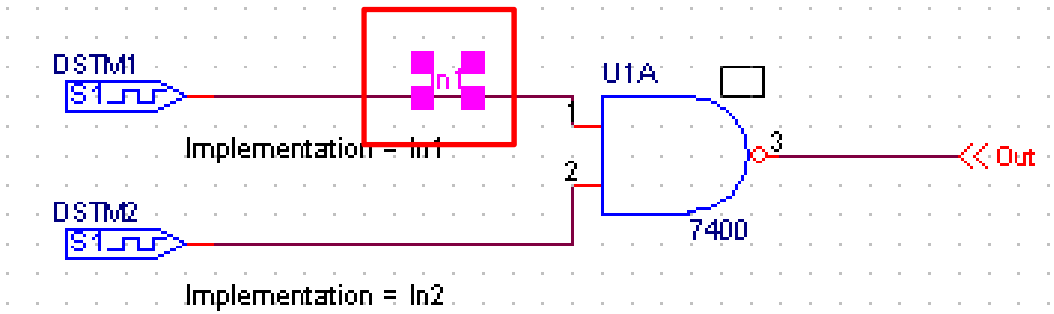

Capture CIS
Edit View Place Macro PSpice Accessories Optior
Part... Shift+P
Parameterized Part...
Database Part Shift+Z
Wire Shift+W
Bus Shift+B
Junction Shift+J
Bus Entry Shift+E
Net Alias... Shift+N
Power... Shift+F
Ground... Shift+G
Off-Page Connector...
PAGELEF
C:₩Docum.
Analog or Mix
File
Design F

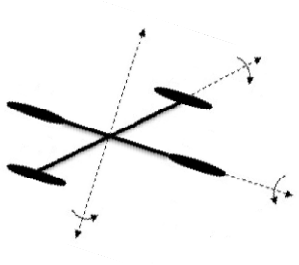

N1
PWR

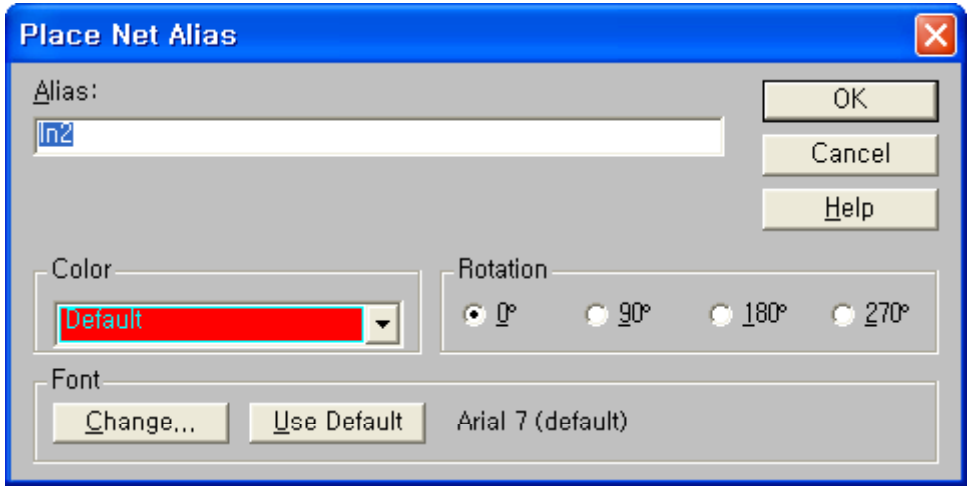


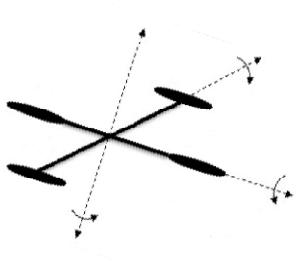

Place Net Alias
Alias:
In1
OK
Cancel
Help
Color
Default
Rotation
0°
90°
180°
270°
Font
Change...
Use Default
Arial 7 (default)

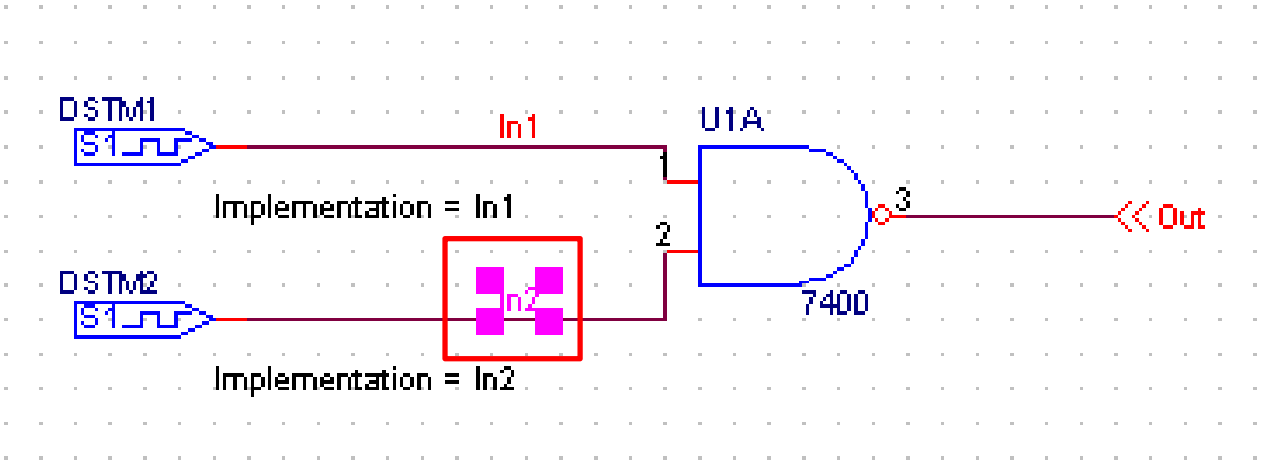


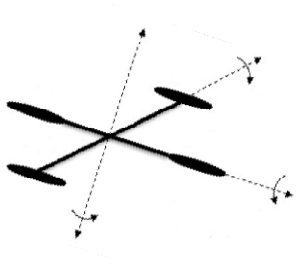

DSTM1
S1
In1
Implementation = In1
U1A
1
2
3
Out
DSTM2
S1
7400
Implementation = In2

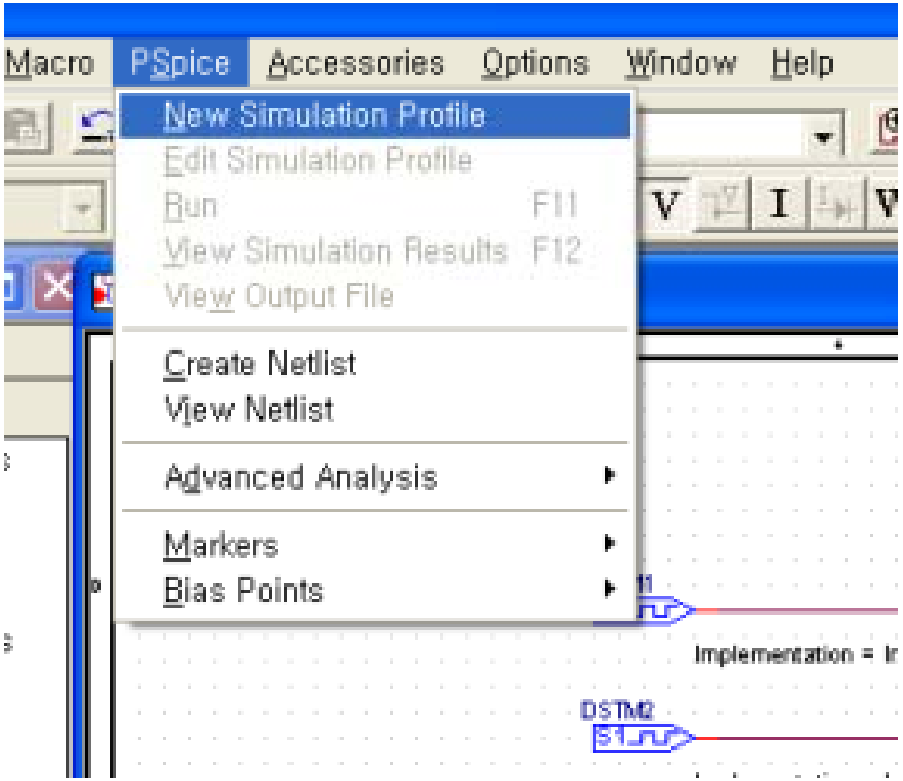


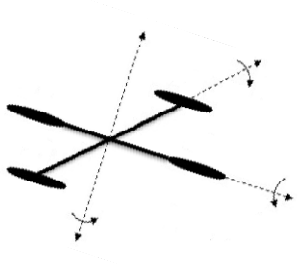

Place Net Alias
Alias:
In2
OK
Cancel
Help
Color
Default
Rotation
0°
90°
180°
270°
Font
Change...
Use Default
Arial 7 (default)

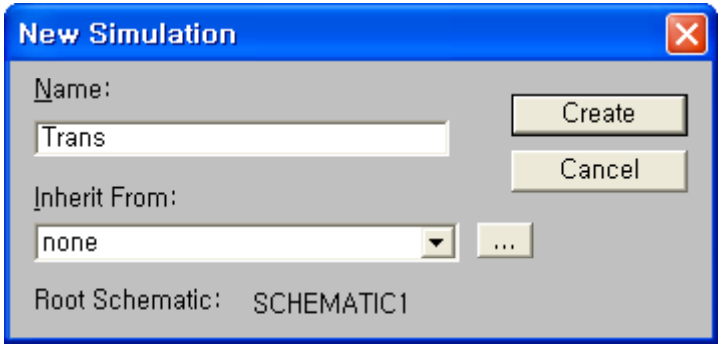


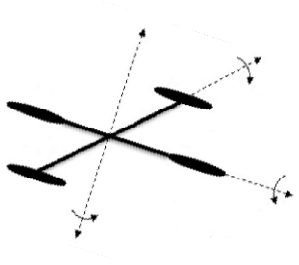

DSTM1
S1
In1
U1A
1
Implementation = In1
2
3
Out
DSTM2
S1
In2
7400
Implementation = In2

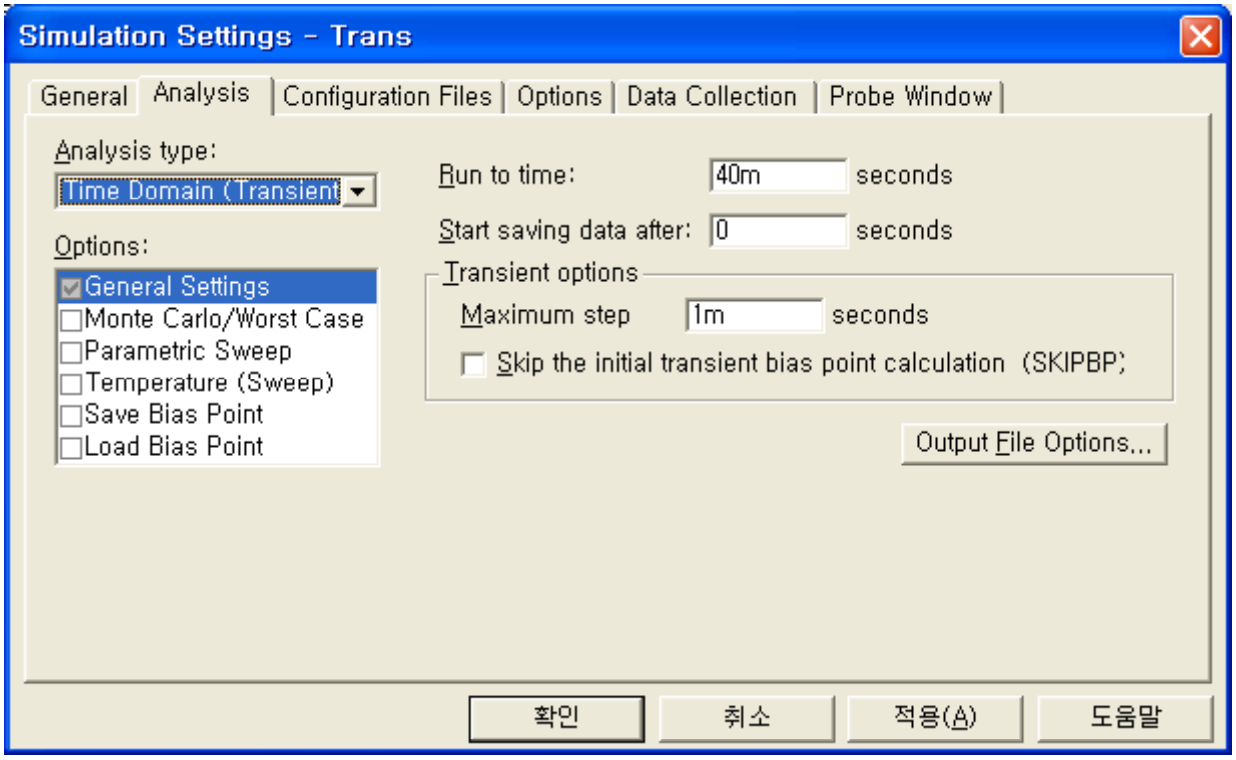


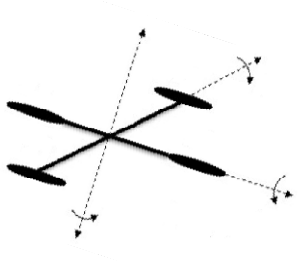

Macro
PSpice
Accessories
Options
Window
Help
New Simulation Profile
Edit Simulation Profile
Run F11
View Simulation Results F12
View Output File
Create Netlist
View Netlist
Advanced Analysis
Markers
Bias Points
V
I
Implementation = Ir
DSTM2
S1

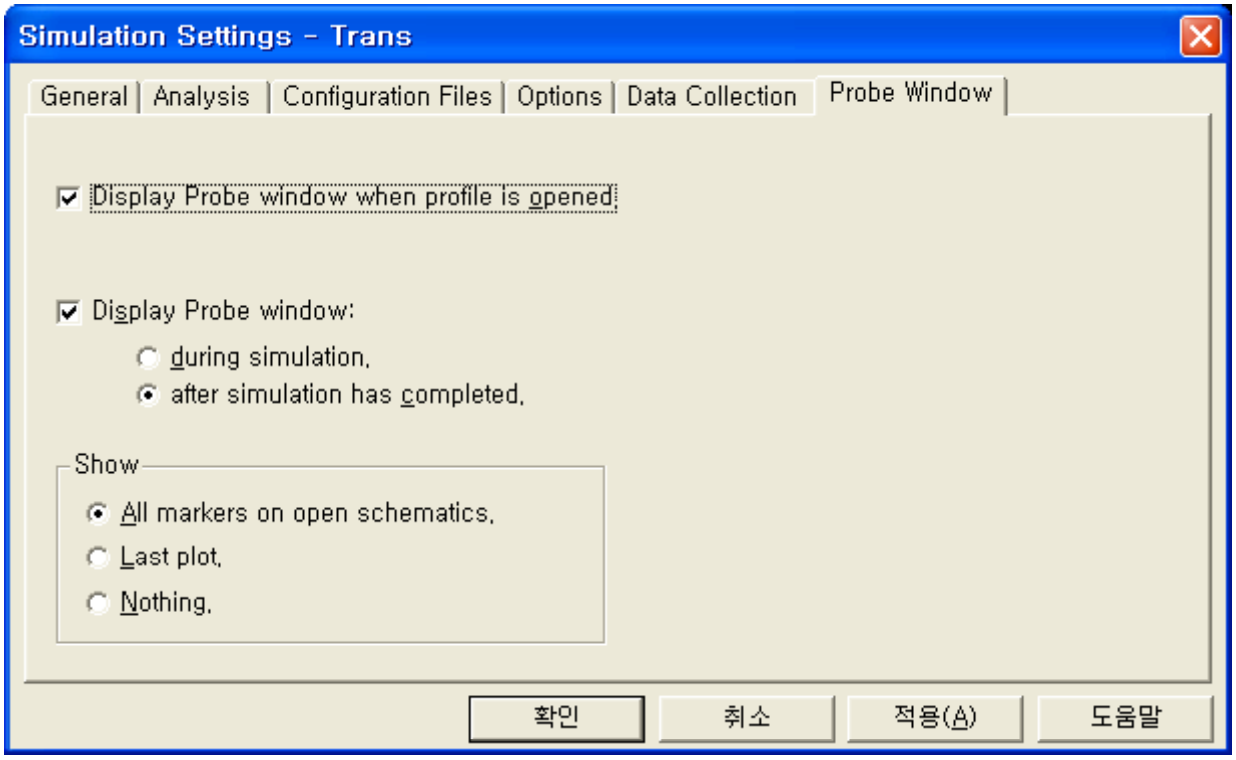


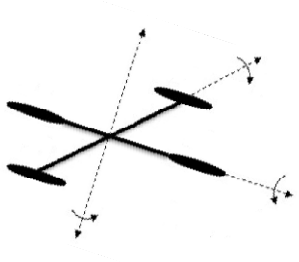

New Simulation
Name:
Trans
Create
Cancel
Inherit From:
none
...
Root Schematic:
SCHEMATIC1

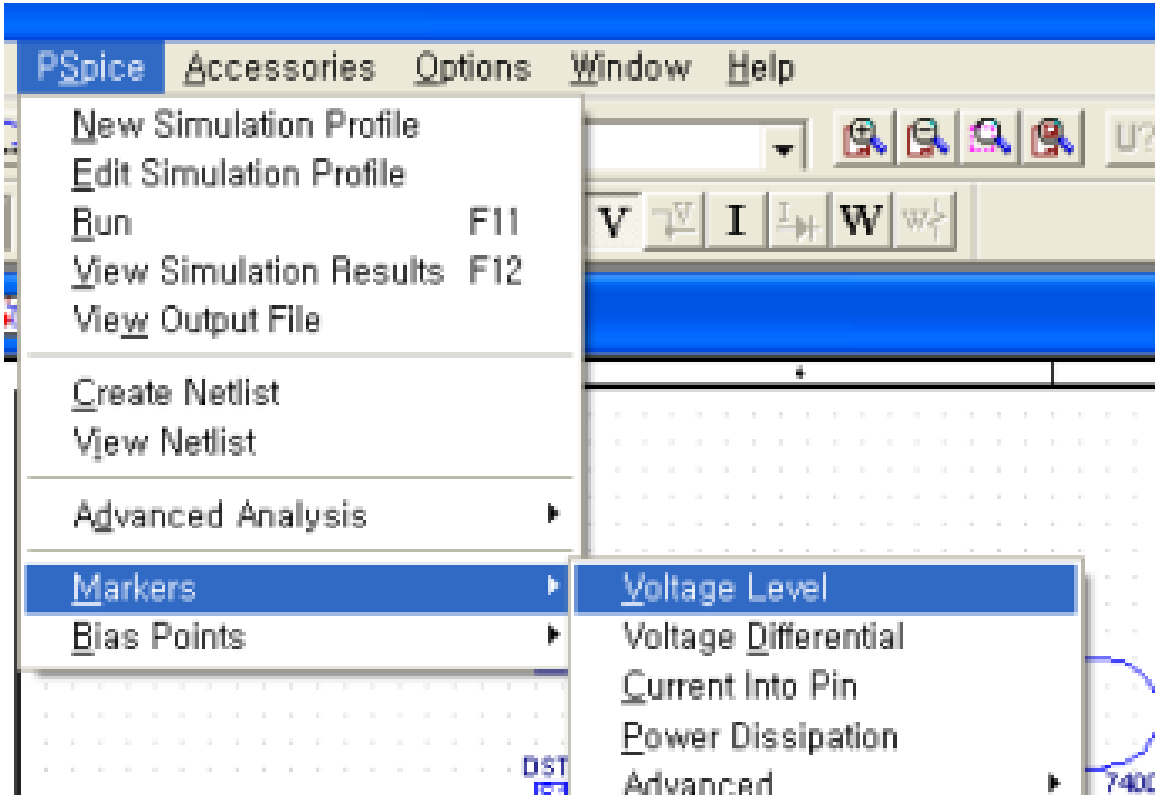


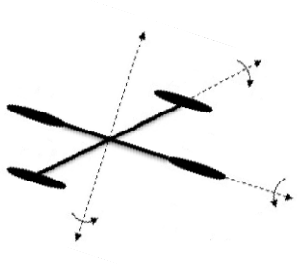

Simulation Settings - Trans
General
Analysis
Configuration Files
Options
Data Collection
Probe Window
Analysis type:
Time Domain (Transient)
Options:
General Settings
Monte Carlo/Worst Case
Parametric Sweep
Temperature (Sweep)
Save Bias Point
Load Bias Point
Run to time:
40m
seconds
Start saving data after:
0
seconds
Transient options
Maximum step
1m
seconds
Skip the initial transient bias point calculation (SKIPBP)
Output File Options...
확인
취소
적용(A)
도움말

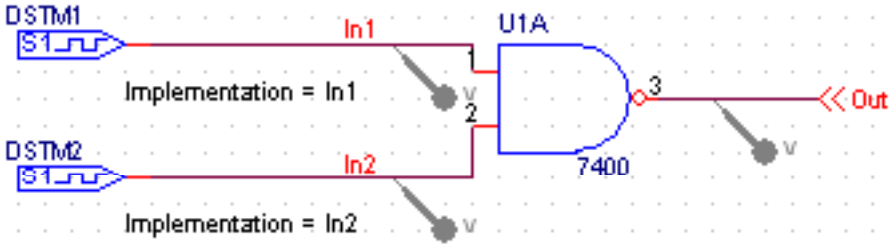


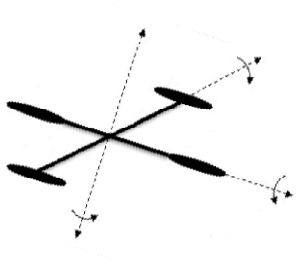

Simulation Settings - Trans
General
Analysis
Configuration Files
Options
Data Collection
Probe Window
Display Probe window when profile is opened
Display Probe window:
during simulation.
after simulation has completed.
Show
All markers on open schematics.
Last plot.
Nothing.
확인
취소
적용(A)
도움말

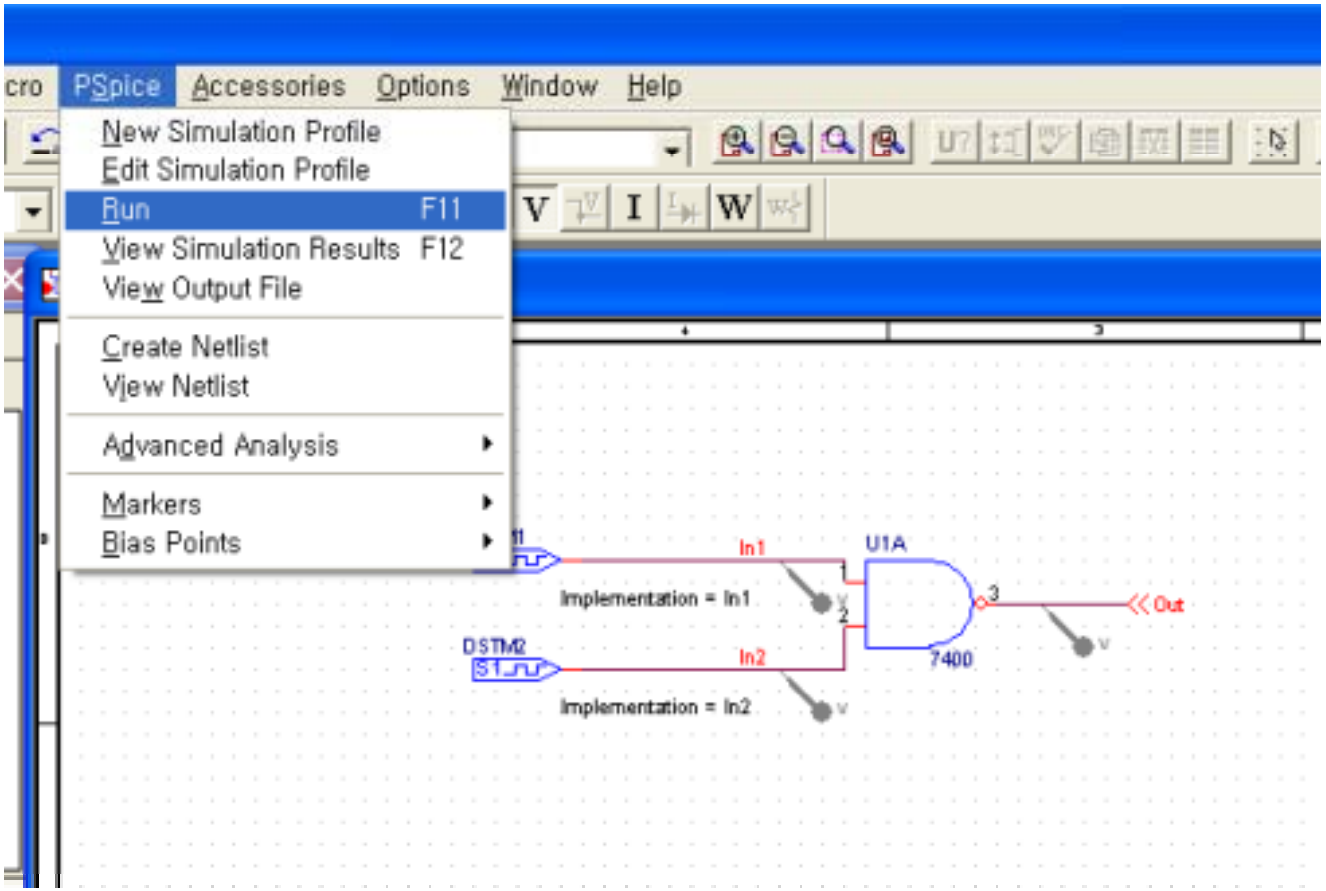


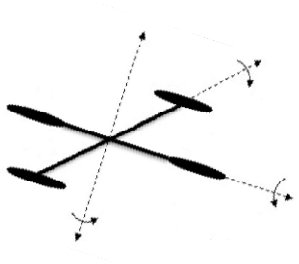

PSpice
Accessories
Options
Window
Help
New Simulation Profile
Edit Simulation Profile
Run F11
View Simulation Results F12
View Output File
Create Netlist
View Netlist
Advanced Analysis
Markers
Bias Points
Voltage Level
Voltage Differential
Current Into Pin
Power Dissipation
Advanced

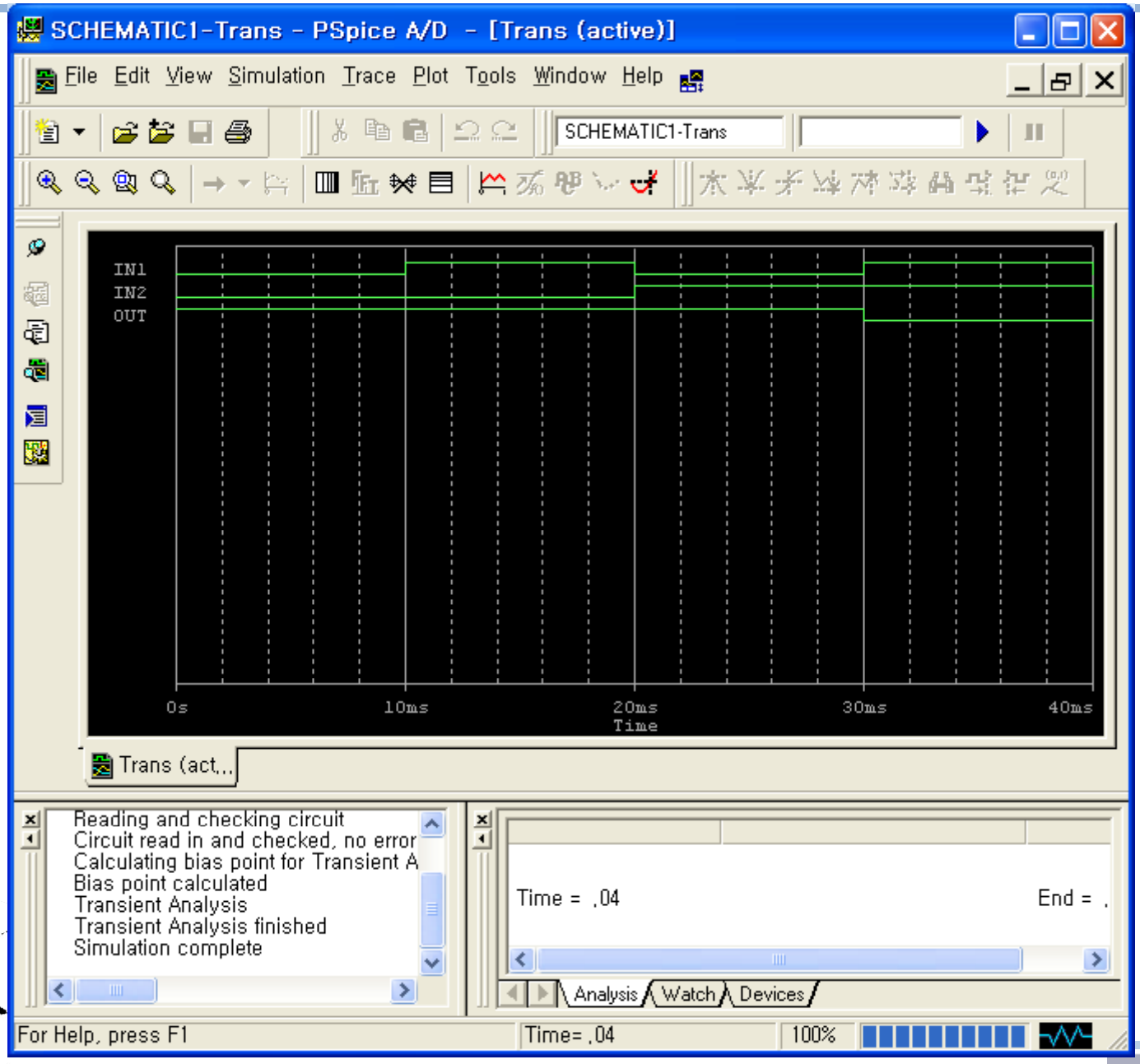



DSTM1
S1
In1
U1A
1
Implementation = In1
2
DSTM2
S1
In2
3
Out
7400
Implementation = In2




cro
PSpice
Accessories
Options
Window
Help
New Simulation Profile
Edit Simulation Profile
Run F11
View Simulation Results F12
View Output File
Create Netlist
View Netlist
Advanced Analysis
Markers
Bias Points
In1
U1A
Implementation = In1
Out
DSTM2
S1
In2
7400
Implementation = In2




SCHEMATIC1-Trans - PSpice A/D - [Trans (active)]
File Edit View Simulation Trace Plot Tools Window Help
SCHEMATIC1-Trans
IN1
IN2
OUT
0s
10ms
20ms
30ms
40ms
Time
Trans (act...
Reading and checking circuit
Circuit read in and checked, no error
Calculating bias point for Transient A
Bias point calculated
Transient Analysis
Transient Analysis finished
Simulation complete
Time = .04
End = .
Analysis
Watch
Devices
For Help, press F1
Time= .04
100%